In a response filed November 18, 2003, Applicants distinguished the present invention from Ohie by stating that Ohie, at a minimum, does not disclose a third bonding wire for connecting the third bonding pad on the second semiconductor chip with the inner lead portion of the first lead. It was also pointed out that Fig. 18 of Ohie shows a first bonding wire 7 which connects a first bonding pad on a first semiconductor chip with the inner lead of a first lead. A plurality of second bonding wires 17 connect plural second bonding pads on the first semiconductor chip with inner lead portions of plural second leads. However, there is no third bonding wire 17 which connects the third bonding pad on the second semiconductor chip with the inner lead portion of the first lead. In other words, none of the inner lead portions of the first leads are connected to both a bonding wire from the first semiconductor chip and a bonding wire from the second semiconductor chip.

The Examiner apparently was persuaded by Applicants' argument, but now relies upon a newly cited patent to Loder et al. The Examiner contends that Loder et al shows a third bonding wire (28 between 24 and 26) on page 3, line 16-19 of the Office Action. However, this third bonding wire 28 does not contact the first lead (for example, 22). In addition,

Loder et al disclose a connection that excludes contact between the third pad (24) of the second chip (14) and the first lead (22)(see column 2, lines 42-49). Therefore, it is submitted that the attempt at combination of references still fails to raise a *prime facia* case of unpatentability.

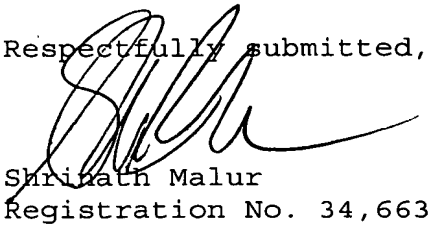
In order to assist the Examiner's understanding of the presently claimed invention, Applicants have attached, as Appendix A, a sketch of Applicants' claim 1 on a page from Ohie's patent containing Figs. 16, 17 and 18. As shown in this sketch, a signal interconnection between a control chip and a memory chip can be achieved by selecting a single lead of a lead frame. This obviates the need for various kinds of lead frames and/or a special control chip having extra bonding pads. As such, the overall cost of the package can be reduced. The Examiner is hereby invited to contact the undersigned with any questions in order to expedite prosecution of the application.

Conclusion

In view of the foregoing amendments and remarks, Applicants contend that the above-identified application is

now in condition for allowance. Accordingly, reconsideration and reexamination are respectfully requested.

Respectfully submitted,



Shrinath Malur
Registration No. 34,663
Attorney for Applicants

MATTINGLY, STANGER & MALUR
1800 Diagonal Rd., Suite 370
Alexandria, Virginia 22314
(703) 684-1120
Date: July 14, 2004

APPENDIX A

Material 1

FIG. 16
(PRIOR ART)

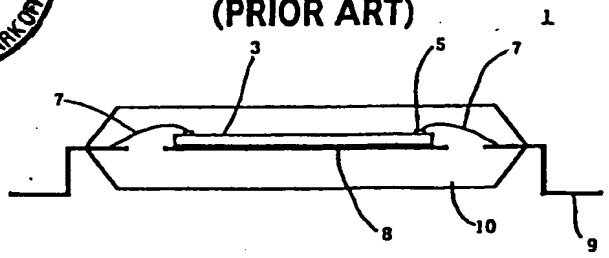
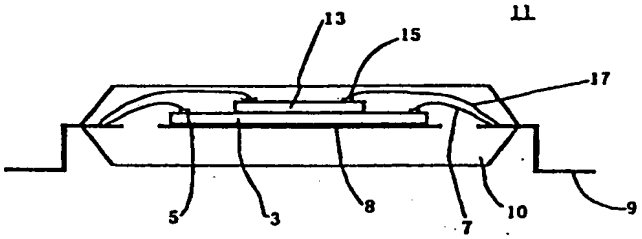


FIG. 17
(PRIOR ART)



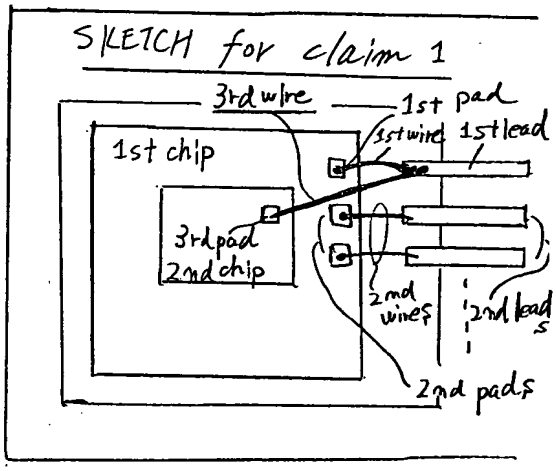


FIG. 18
(PRIOR ART)